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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR		ATTORNEY DOCKET NO.
08/707,694	09/04/96	RANGASAYEE	K	64.663-063

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EXAMINER	
BUTLER, D	
ART UNIT	**PAPER NUMBER**
2787	10

DATE MAILED: 02/01/00

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary	Application No. 707694	Applicant(s)	
	Examiner Butler	Group Art Unit	

—The MAILING DATE of this communication appears on the cover sheet beneath the correspondence address—

Period for Response

A SHORTENED STATUTORY PERIOD FOR RESPONSE IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a response be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for response specified above is less than thirty (30) days, a response within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for response is specified above, such period shall, by default, expire SIX (6) MONTHS from the mailing date of this communication .
- Failure to respond within the set or extended period for response will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).

Status

☒ Responsive to communication(s) filed on 8-10-98.

☒ This action is **FINAL.**

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 1 1; 453 O.G. 213.

Disposition of Claims

☒ Claim(s) 1-20 is/are pending in the application.

Of the above claim(s)____ is/are withdrawn from consideration.

☐ Claim(s)____ is/are allowed.

☒ Claim(s) 1-20 is/are rejected.

☐ Claim(s)____ is/are objected to.

☐ Claim(s)____ are subject to restriction or election requirement.

Application Papers

☐ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The proposed drawing correction, filed on____ is ☐ approved ☐ disapproved.

☐ The drawing(s) filed on____ is/are objected to by the Examiner.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119 (a)-(d)

☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 11 9(a)-(d).

☐ All ☐ Some* ☐ None of the CERTIFIED copies of the priority documents have been

☐ received.

☐ received in Application No. (Series Code/Serial Number)____.

☐ received in this national stage application from the International Bureau (PCT Rule 1 7.2(a)).

*Certified copies not received:____.

Attachment(s)

☒ Information Disclosure Statement(s), PTO-1449, Paper No(s). 8-10-98

☐ Interview Summary, PTO-413

☒ Notice of References Cited, PTO-892

☐ Notice of Informal Patent Application, PTO-152

☐ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Other____

Office Action Summary

1. This action is in response to paper number 9, Amendment A, which was received on August 10, 1998. Claims 1-20 are pending.

2. Regarding the applications cited on applicant"s IDS received 8-10-98, the examiner has considered the Patents that have issued from applications 08/626043 and 08/587659. Application 08/699048 is abandoned and has not been considered because it is not prior art.

3. The text of those sections of Title 35, US Code not included in this action can be found in a prior Office Action.

4. Claims 6-9, 11 and 17-20 are rejected under 35 USC 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claim 11, this claim recites desired functional results without reciting any structural elements capable of performing the purported functions. Therefore, the claim is unclear as to what performs the recited functions.

Regarding claim 6, the phrase "said output frequencies" lacks proper antecedent basis.

Regarding claim 17, the phrase "the impedance" lacks proper antecedent basis.

Claims 7-9 and 18-20 are unclear as to whether one or more reference clock frequencies can be selected because in the case when only one reference clock frequency is present in the system there is nothing to select.

5. Claims 11, 5, 14 and 17 are rejected under 35 USC § 112, first paragraph, as containing subject matter which was not

described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Regarding claim 11, the specification as filed does not properly describe reducing the input and output delay to zero in response to programming inputs which are also used to program the output frequency.

Regarding claims 5, 14 and 17, the specification as filed does not properly describe providing programming inputs which are used to adjust an impedance.

6. Claims 11, 5, 14 and 17 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Regarding claim 11, the specification does not provide an enabling disclosure of how to make and/or use a programmable device in which the input and output delay is reduced to zero in response to programming inputs which are also used to program the output frequency. The examiner could find no description in the specification that would enable one of ordinary skill in the art to make and/or use the claimed elements\functions without undue experimentation. Regarding claims 5, 14 and 17, the specification does not provide an enabling disclosure of how to make and/or use programming inputs which are used to adjust an impedance. The only known description of adjusting an impedance is at page 10,

lines 7-9. This description merely states that the clock outputs have an output impedance that may be adjusted to match the impedance of an external device. There is not the slightest hint of including programmable inputs for adjusting an output impedance. The specification is not even clear whether the adjustment is performed during the design of the circuit/device or after it has been designed. The examiner could find no description in the specification that would enable one of ordinary skill in the art to make and/or use the claimed elements\functions without undue experimentation.

7. Claims 1-4, 6, 12-13 and 15-16 are rejected under 35 USC 102(b) as being anticipated by Davis et al., U.S. Patent 4,893,271.

Per claims 1, 12 and 15:

A) Davis et al teach the following claimed items:

1. means/first circuit for storing programmable information with Frequency Control Register 240 or RAM 252 or ROM 250 of figure 3 and at column 7, lines 41-55;

2. means/second circuit for (capable of) providing a plurality of output clocks in response to a reference clock frequency each capable of oscillating at a different one of a plurality of frequencies with Frequency Synthesized Timing Generator 200 of figures 2, 3 and 4, with Timing Selector Circuit 206 of figures 3 and 4, with Timer Input Selector 218 of figure 3, at column 8, lines 6-53 and at column 9, lines 7-43.

Per claims 2, 13 and 16:

Davis et al teach providing a plurality of output clocks which are individually programmable to a plurality of frequencies at column 9, lines 33-55.

Per claim 3:

See the rejection of claim 12.

Per claim 4:

Davis et al teach the output clock being accessible through one or more input/output pins with pins 110 and/or 112 and/or 114 of figures 2 and 3 and at column 5, line 56 - column 6, line 2.

Per claim 6:

See the rejection of claim 12.

8. Claims 5, 7, 10-11, 14 and 17-20 are rejected under 35 USC 103 as being unpatentable over Davis et al., U.S. Patent 4,893,271, in view of Hotta et al., U.S. Patent 5,506,982.

Per claims 5, 11, 14 and 17:

Claims 5, 11, 14 and 17 recite desired functional results without reciting any structural elements capable of performing the purported functions. Therefore, these recited functions are not deemed to carry any patentable weight. In addition, the recited functions are well known in the timing art as described by Hotta at column 3, line 63 - column 4, line 12 and at column 5, line 65 - column 6, line 30 and would have been obvious to one of ordinary skill in the art.

Per claims 7-9:

Davis et al teach the reference clock comprising one or more clock frequencies with the reference clock output on line

202 of figures 2, 3 and 4. Davis teaches that it is known to select from one or more reference frequencies with Variable Divider 106 of figure 1b which is functionally equivalent to selecting from one or more reference frequencies using a multiplexer. In addition, a multiplexer is a well known device used for selecting one of a plurality of signals. Hotta describes that it is well known to generate both internal and external reference clock signals using clock buffering at column 4, lines 22-30.

Per claim 10:

Davis et al teach the claimed elements as described above in the rejection of claim 12. The claim seems to differ from Davis et al in that Davis et al fails to explicitly teach providing a programmable logic device comprising the elements of claim 12 as claimed. However, Hotta teaches that it is known to provide a programmable logic device comprising the elements of claim 12 as set forth with figures 1, 8 and 16, at column 9, lines 22-50 and at column 11, lines 13-39. It would have been obvious to one having ordinary skill in the data processing art at the time the invention was made to provide a programmable logic device comprising the elements of claim 12, as taught by Hotta, in order to provide a PLA which is programmably controlled by a phase locked loop multiplied clock signal. One of ordinary skill in the art would have been motivated to combine Davis and Hotta because of Hotta's suggestion at column 1, lines 22-30, at column 5, lines 4-23, at column 9, lines 46-50 and

with figures 1, 8, 16 and 23. It would have been obvious for one of ordinary skill in the art to combine Davis and Hotta because they are both directed to the problem of generating a plurality of phase locked clock signals for a programmable logic device.

Per claims 18-20:

Claims 18-20 recite obvious variations of well known clock signal generation procedures and would have been obvious to one of ordinary skill in the art. Hotta describes that it is well known to generate both internal and external reference clock signals using clock buffering at column 4, lines 22-30.

9. Claims 1-2, 4, 6-9 and 12-13 are rejected under 35 USC 102(e) as being anticipated by Weiss et al., U.S. Patent 5,774,703.

Per claims 1 and 12:

A) Weiss et al teach the following claimed items:

1. means/first circuit for storing programmable information with Registers 200, 250 and 300 of figure 1;

2. means/second circuit for (capable of) providing a plurality of output clocks in response to a reference clock frequency each capable of oscillating at a different one of a plurality of frequencies with figures 4 and 5 and at column 5, line 47 - column 8, line 21.

Per claims 2, 4, 6-9 and 13:

Weiss teaches all of the claimed elements with figures 1 and 4-5 and at column 5, line 47 - column 8, line 21.

10. Applicant's remarks have been considered and have been addressed in the above art rejections.

11. Applicant's amendment necessitated the new grounds of rejection. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR § 1.136(a).

A SHORTENED STATUTORY PERIOD FOR RESPONSE TO THIS FINAL ACTION IS SET TO EXPIRE THREE MONTHS FROM THE DATE OF THIS ACTION. IN THE EVENT A FIRST RESPONSE IS FILED WITHIN TWO MONTHS OF THE MAILING DATE OF THIS FINAL ACTION AND THE ADVISORY ACTION IS NOT MAILED UNTIL AFTER THE END OF THE THREE-MONTH SHORTENED STATUTORY PERIOD, THEN THE SHORTENED STATUTORY PERIOD WILL EXPIRE ON THE DATE THE ADVISORY ACTION IS MAILED, AND ANY EXTENSION FEE PURSUANT TO 37 CFR § 1.136(a) WILL BE CALCULATED FROM THE MAILING DATE OF THE ADVISORY ACTION. IN NO EVENT WILL THE STATUTORY PERIOD FOR RESPONSE EXPIRE LATER THAN SIX MONTHS FROM THE DATE OF THIS FINAL ACTION.

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dennis M. Butler whose telephone number is (703) 305-9663. The examiner can normally be reached on Monday-Friday from 9:30 AM to 6:00 PM.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 305-3900.

Dennis M. Butler
January 28, 2000

Dennis M. Butler
Primary Examiner
Group 2780